ELECTION WITHOUT TRAVERSE BETWEEN GROUP I AND GROUP II

Applicants elect without traverse Group II, recited in Claims 1-9 relating to a semiconductor structure, and Claims 10-12 relating to a pad area apparatus for a semiconductor structure.

IN THE CLAIMS

Please cancel Claims 13-21 without prejudice. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Original) A semiconductor structure comprising:
a pad area; and
an active device of said semiconductor structure disposed below said pad area.

2. (Original) The semiconductor structure as recited in Claim 1 wherein said active component comprises a transistor.

3. (Original) The semiconductor structure as recited in Claim 1 wherein a component of said
semiconductor structure performs a logic function.

4. (Original) The semiconductor structure as recited in Claim 1 wherein a component of said
semiconductor structure performs a memory function.

5. (Original) The semiconductor structure as recited in Claim 1 wherein said active device comprises a first device, said semiconductor structure further comprising:
a non-pad area bounded at least in part by said pad area; and
a second device disposed within said non-pad area.

6. (Original) The semiconductor structure as recited in Claim 5 wherein said first and said second devices perform a similar function.

7. (Original) The semiconductor structure as recited in Claim 1 wherein said pad area comprises:

a substrate;

a first layer of metal disposed above said substrate wherein said active device is disposed below said first layer of metal;

a second layer of metal disposed above said first layer of metal.

8. (Original) The semiconductor structure as recited in Claim 7 further comprising:

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

9. (Original) The semiconductor structure as recited in Claim 7 further comprising a subsequent layer of metal between said first and said second metal layers.

10. (Original) A pad area apparatus for a semiconductor structure comprising:

a substrate;

a first layer of metal disposed above said substrate;

a second layer of metal disposed above said first layer of metal; and

an active component wherein said active component is disposed within said substrate.

11. (Original) The pad area apparatus as recited in Claim 10 further comprising:

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

12. (Original) The pad area apparatus as recited in Claim 10 further comprising a subsequent layer of metal between said first and said second metal layers.

13-21. (Cancelled)